IN THE SPECIFICATION

Please replace the paragraphs below with the amended paragraphs as follows:

On page 9, beginning lines 18-23:

For example, messages between the switch controller SWC-A 310_A and the primary head-end controller 130_1 may be sent bi-directionally via signal path 317_A, through the first Ethernet switch 144_1, and then through signal path 119_1. Similarly, messages between the switch controller SWC_B 310_B and the primary head-end controller 130_1 ~~119_4~~ may be sent bi-directionally via signal paths 317_B, through the second Ethernet switch 144_2, and then through signal path 119_2 ~~paths 119_V~~. Likewise, communications between the secondary switch controller SWC-B 310_B and the secondary head-end controller 130_2 may be provided in a similar manner, as shown in FIG. 1.

B1

On page 11, beginning lines 17-29:

During operation, in an exemplary embodiment I/O port 1 320_1 pings I/O port 2 320_2 first, then 5 milliseconds later pings I/O port 3 320_3, then 5 milliseconds later pings I/O port 4 320_4, and continues in this manner through I/O port 16 320_{16} before repeating the cycle, i.e., in a "round robin" process. [[.]] In addition, the other I/O ports 2 through 16 320_2 through 320_{16} are likewise pinging one another in a similar manner. Furthermore, a few fractions of a millisecond after each ping is sent, 16 acknowledgements are being sent from the recipient I/O port 320 back to the originating I/O port. Once an I/O port has consecutively pinged the other 15 I/O ports, a cycle has been completed. Thus, during each 5-millisecond interval, 16 individual pings and corresponding acknowledgements are being passed through the switch matrix 306_A of the primary switch controller 310_A. Therefore, during the course of one complete cycle (i.e., 75 milliseconds) the switch matrix 306_A functions as a 16x16 array, and will have transferred 240 pings and 240 acknowledgement signals.

B2